

Substitute Form PTO-1449 (Modified)		U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-320001	Application No. 09/811,995
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant Matthew J. Adiletta et al. Filing Date March 19, 2001		
				Group Art Unit 2183

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Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
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Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation
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/AL/	DN	0 130 381	01/1985	Europe			
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/AL/	DU	Bowden, Romilly, "What is HART?" Romilly's HART® and Fieldbus Web Site, 3 pages, (1997). <URL: http://www.romilly.co.uk/whathart.htm >
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/AL/	DW	Hennessy et al., <i>Computer Organization and Design: The Hardware/Software Interface</i> , Morgan Kaufman Publishers, pp. 116-119, 181-182, 225-227, 447-449, 466-470, 476-482, 510-519, 712, (1998).

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	DZ	Hirata, H., et al., "An Elementary Processor Architecture with Simultaneous Instruction Issuing from Multiple Threads", <i>Proc. 19th Annual International Symposium on Computer Architecture, ACM & IEEE-CS</i> , 20(2):136-145, May 1992.	
	EA	Intel, "IA-64 Application Developer's Architecture Guide," Rev.1.0, pp. 2-2, 2-3, 3-1, 7-165, C-4, and C-23, May 1999.	
	EB	Jung, G., et al., "Flexible Register Window Structure for Multi-Tasking", <i>Proc. 24th Annual Hawaii International Conference on System Sciences</i> , vol. 1, pp. 110-116, (1991).	
	EC	Koch, G., et al., "Breakpoints and Breakpoint Detection in Source Level Emulation", <i>Proc. 19th International Symposium on System Synthesis (ISSS '96)</i> , IEEE, pp. 26-31 (1996).	
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/AL/	EG	Paver, et al., "Register Locking in an Asynchronous Microprocessor", <i>IEEE</i> , pp. 351-355, (1992).	
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	EI	Quammen, D., et al., "Flexible Register Management for Sequential Programs", <i>IEEE Proc. of the Annual International Symposium on Computer Architecture</i> , Toronto, May 27-30, 1991, vol. SYMP. 18, pp. 320-329.	
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